REMARKS

Following entry of the above amendment, claims 1-14, 21-25 and 27 will be pending. Claim 1 has been amended to include the feature: "a second dielectric layer separating the second gate from the SOI substrate, the second dielectric layer having a relative permittivity less than the first dielectric layer." Claim 2 has been amended to include the feature: "the second work function is less than the work function of the first gate." Claim 24 has been amended to provide antecedent basis for the term "liner" without change in scope.

I. ALLOWABLE SUBJECT MATTER

Applicants acknowledge with appreciation the Examiner's indication that claims 10-14, 24 and 25 are allowed.

II. REJECTION OF CLAIMS UNDER 35 USC §103(a)

Claims 1, 4-8, 22, 23 and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee, U.S. Patent No. 5,600,168 ("Lee"), in view of Chooi et al., U.S. Patent No. 6,486,080 B2[1], ("Chooi"). Claims 2, 3 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Chooi as applied to claim 1, and further in view of Mandelman et al., U.S. Patent No. 6,097,070 ("Mandelman"). Claim 9 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Chooi as applied to claim 1, and further in view of Liu et al., U.S. Patent No. 6,218,276 B1 ("Liu"). Withdrawal of the rejections is respectfully requested for at least the following reasons.

Referring now to FIG. 4h of Lee, reproduced below for the Examiner's convenience, Lee discloses a MOSFET having an LDD structure formed on a p-type semiconductor substrate 1. Lee also discloses first gate insulation films 16 on both ends of an upper part of the semiconductor substrate region between low density impurity regions 24. Lee further discloses a

[1] The rejection on page 2 of the Office Action (OA) cites Chooi et al. as U.S. Patent No. 6,486,020, line 2 of paragraph 4. Chooi is actually U.S. Patent No. 6,486,080 as cited by the Examiner on the Notice of References Cited form attached to the OA. Therefore the rejection is being treated as a combination of Lee and Chooi et al. (U.S. Patent No. 6,486,080).

second gate insulation film 18 on the semiconductor substrate region between the ends of first gate insulation films 16. Lee also discloses first conduction layers 17 (annotation added) in the form of side wall spacers on the first gate insulation films 16 and a second conduction layer 21 (annotation added) on the second gate insulation film 18 filling a space formed by and between the first conduction layers 17 of side wall spacers. Additionally, Lee discloses forming a gate pole connecting the first conduction layer 17, the second conduction layer 21, and a third conduction layer 22 which is formed on the first conduction layer 17 and the second conduction layer 21, together. See, for example, Col 4, lines 10-36).

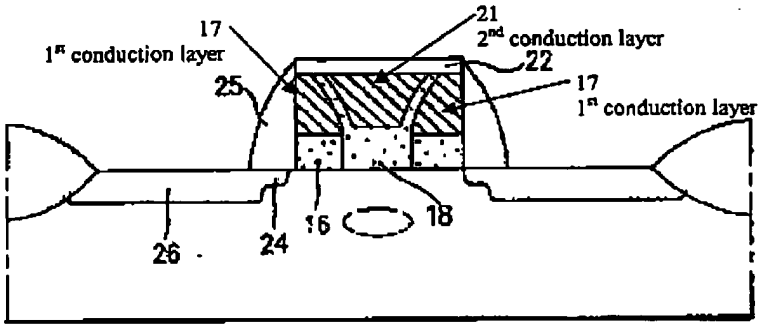

Figure 1: FIG. 4h of Lee

Lee does not disclose, as indicated by the Examiner in the OA, a device comprising an SOI substrate, nor a device including a high dielectric constant gate insulation region with a dielectric constant greater than silicon dioxide. Further, Lee does not disclose a second dielectric layer separating the second conduction layer from an SOI substrate, the second dielectric layer having a relative permittivity less than the first dielectric layer.

Claim 1 as amended includes, *inter alia*, the features "a first dielectric layer separating the first gate from the SOI substrate, the first dielectric layer having a relative permittivity greater than SiO_2, and a second dielectric layer separating the second gate from the SOI substrate, the second dielectric layer having a relative permittivity less than the first dielectric layer. In contrast, Lee discloses a thermal oxidation process is performed to form a second gate oxidation film 18 as a gate insulation film on the substrate area exposed by the etching of the first gate

oxidation film 16 and the first conduction layers 17. The second gate oxidation film 18 is formed thicker than the first gate oxidation film 16. See, for example, Col 5, lines 16-30. Thus, the relative permittivity of the second gate oxidation film 18 compared to the relative permittivity of the first gate oxidation film 16 is the same since the second gate oxidation film 18 and the first gate oxidation film 16 are made of the same material, i.e., silicon dioxide. See, for example, Col 5, lines 3-6. However, the electrical equivalent thickness of the second gate oxidation film 18 is greater than the electrical equivalent thickness of the first gate oxidation film 16 since the second gate oxidation film 18 is thicker than the first gate oxidation film 16.

Amended claim 1 recites the first dielectric layer separating the first gate from the SOI substrate includes a relative permittivity greater than SiO_2. Further, the second dielectric layer separating the second gate from the SOI substrate includes a relative permittivity less than the first dielectric layer.

Chooi does not make up for the deficiencies of Lee. That is, Chooi does not disclose a first dielectric layer separating the first gate from the SOI substrate includes a relative permittivity greater than SiO_2 and a second dielectric layer separating the second gate from the SOI substrate includes a relative permittivity less than the first dielectric layer. Chooi simply discloses an SOI substrate including a high dielectric constant gate insulation region 18 (hafnium oxide). See, for example, Col. 4, lines 4-20.

If the high dielectric constant gate insulation region 18 disclosed by Chooi replaced the first gate oxidation film 16 and the second gate oxidation film 18 of Lee, the resulting device would not include the features recited in amended claim 1. That is, the resulting device would not include a first dielectric layer separating a first gate from the SOI substrate that includes a relative permittivity greater than SiO_2 and a second dielectric layer separating a second gate from the SOI substrate that includes a relative permittivity less than the first dielectric layer.

Further, if each of the first gate oxidation film 16 and the second gate oxidation film 18 of Lee were replaced with the high dielectric constant gate insulation region 18 disclosed by Chooi with the thicknesses disclosed in Lee, the features of amended claim 1 would still not be achieved. That is, the relative permittivity of the second gate oxidation film 18 compared to the

first gate oxidation film 16 would be the same since the second gate oxidation film 18 and the first gate oxidation film 16 are made of the same material, i.e., hafnium oxide. Similar to Lee described above, the electrical equivalent thickness of the second gate oxidation film 18 would still be greater than the electrical equivalent thickness of the first gate oxidation film 16. In other words, the second gate oxidation film 18 is still electrically thicker than the first gate oxidation film 16.

Therefore, since Lee alone or in combination with Chooi does not teach or suggest one or more of the features as claimed in amended claim 1, claims 4-8, 22, 23 and 27 that depend therefrom are allowable over Lee alone or in combination with Chooi.

With regard to claims 2, 3 and 21, claims 2, 3 and 21 depend from amended claim 1. Mandelman does not make up for the deficiencies of Lee and Chooi alone or in combination as discussed above with regard to amended claim 1. Therefore, since Lee alone or in combination with Chooi and Mandelman does not teach or suggest one or more of the features as claimed in amended claim 1, claims 2, 3 and 21 that depend therefrom are allowable over Lee alone or in combination with Chooi and Mandelman.

With regard to claim 9, claim 9 depends from amended claim 1. Liu does not make up for the deficiencies of Lee and Chooi alone or in combination as discussed above with regard to amended claim 1. Therefore, since Lee alone or in combination with Chooi and Liu does not teach or suggest one or more of the features as claimed in amended claim 1, claim 9 that depends therefrom is allowable over Lee alone or in combination with Chooi and Liu.

III. CONCLUSION

In light of the foregoing, it is respectfully submitted that the present application is in condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present invention.

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Reply Dated June 3, 2004

Any fee(s) resulting from this communication is hereby authorized to be charged to our Deposit Account No. 18-0988; Our Order No. F0537 (AMDSP0429US).

Respectfully submitted,
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